Fig. 1

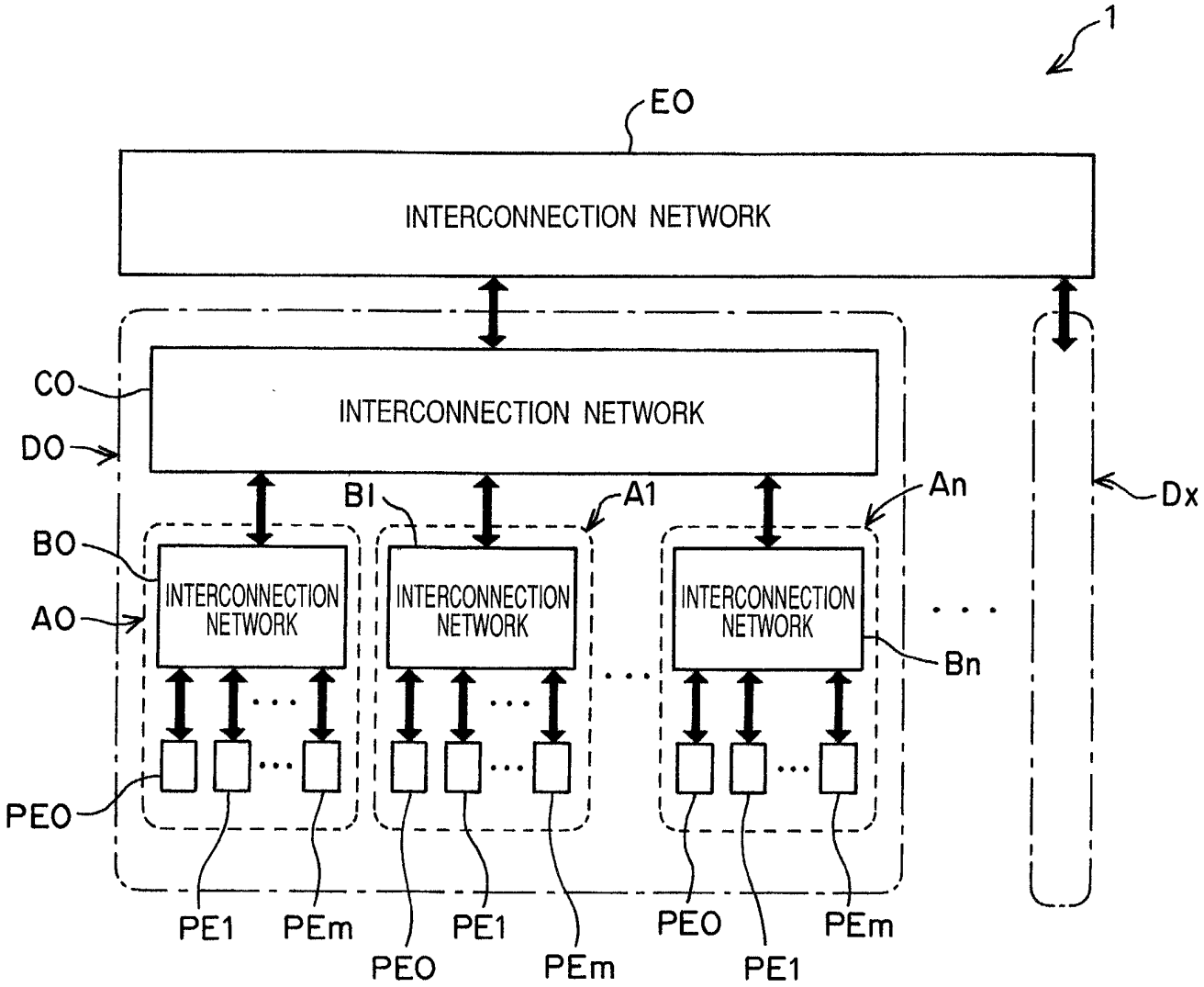
1
EO
INTERCONNECTION NETWORK
CO
DO
INTERCONNECTION NETWORK
BI
A1
An
Dx
BO
AO
INTERCONNECTION NETWORK
INTERCONNECTION NETWORK
INTERCONNECTION NETWORK
Bn
PEO
PE1
PEm
PE1
PEm
PEO
PEO
PEm
PE1

Fig. 2

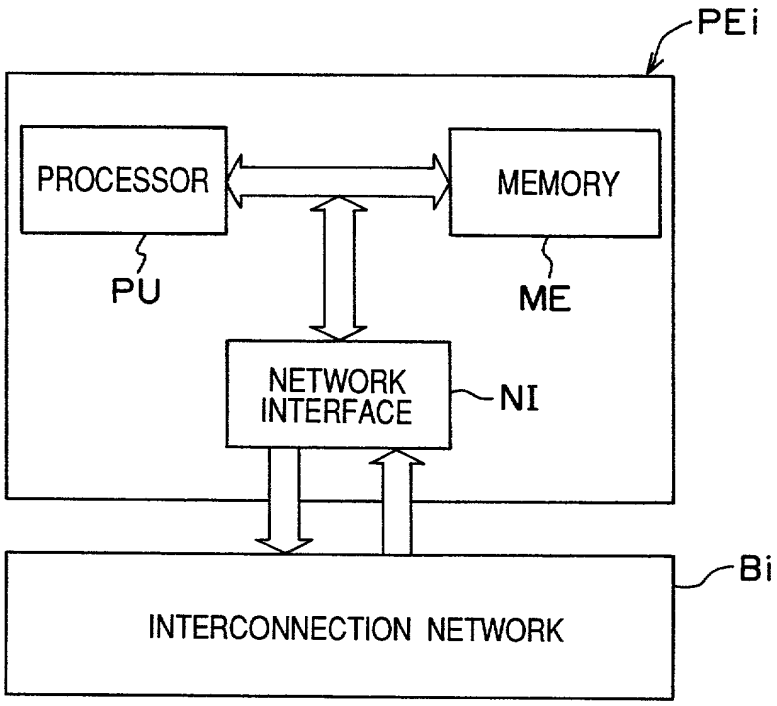
PEi
PROCESSOR
MEMORY
PU
ME
NETWORK INTERFACE
NI
Bi
INTERCONNECTION NETWORK

Fig. 3

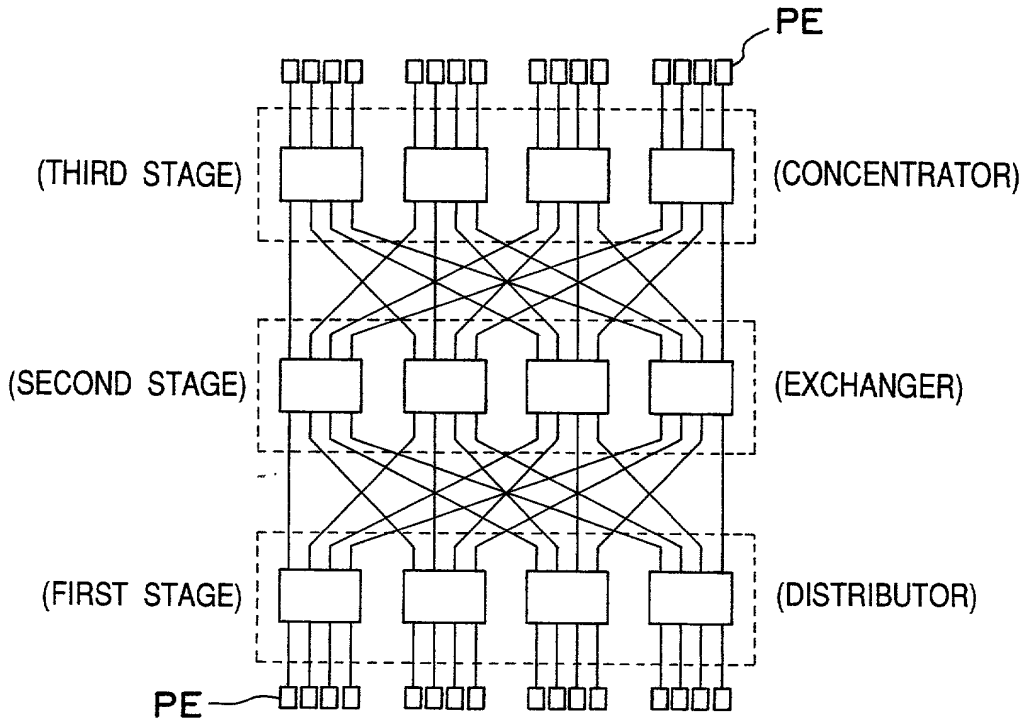
PE
(THIRD STAGE)
(CONCENTRATOR)
(SECOND STAGE)
(EXCHANGER)
(FIRST STAGE)
(DISTRIBUTOR)
PE

Fig.4

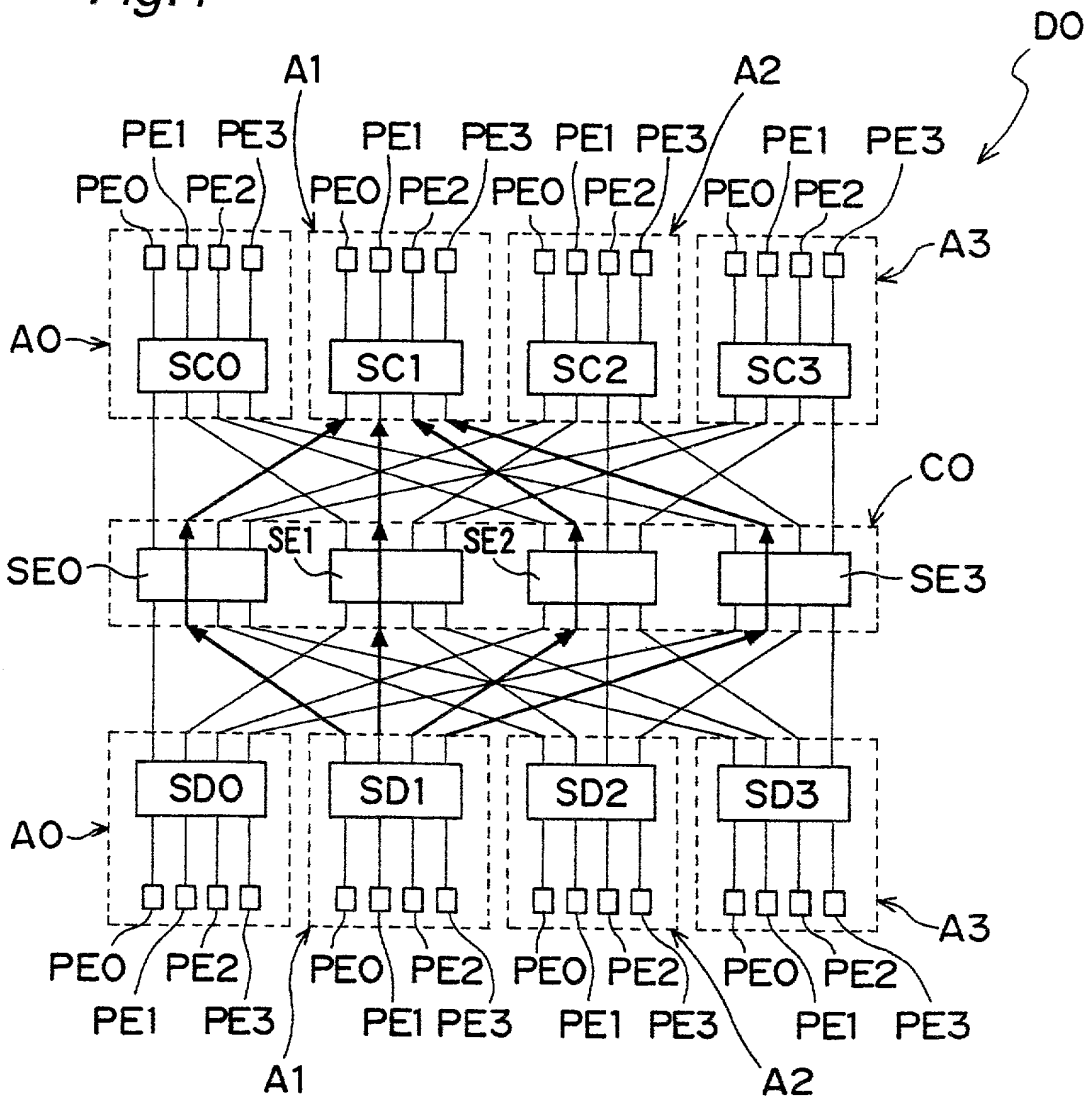
DO
A1
A2
PE1 PE3 PE1 PE3 PE1 PE3 PE1 PE3
PE0 PE2 PE0 PE2 PE0 PE2 PE0 PE2
A3
AO
SC0
SC1
SC2
SC3
CO
SE1
SE2
SEO
SE3
SD0
SD1
SD2
SD3
AO
A3
PE0 PE2 PE0 PE2 PE0 PE2 PE0 PE2
PE1 PE3 PE1 PE3 PE1 PE3 PE1 PE3
A1
A2

Fig.5

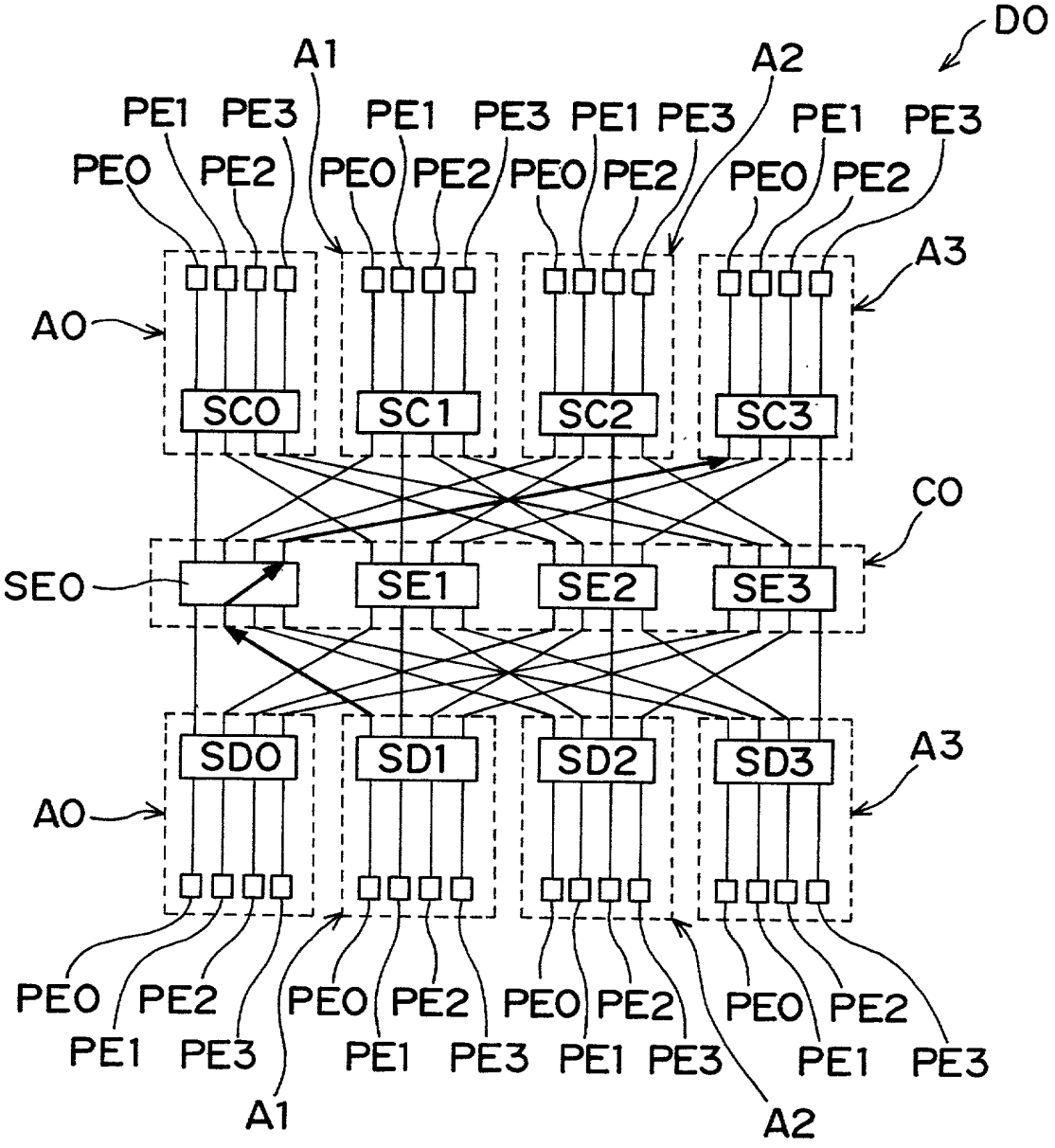
DO
A1
A2
PE1 PE3 PE1 PE3 PE1 PE3 PE1 PE3
PE0 PE2 PE0 PE2 PE0 PE2 PE0 PE2
A3
A0
SC0
SC1
SC2
SC3
CO
SE0
SE1
SE2
SE3
SD0
SD1
SD2
SD3
A3
A0
PE0 PE2 PE0 PE2 PE0 PE2 PE0 PE2
PE1 PE3 PE1 PE3 PE1 PE3 PE1 PE3
A1
A2

Fig.6

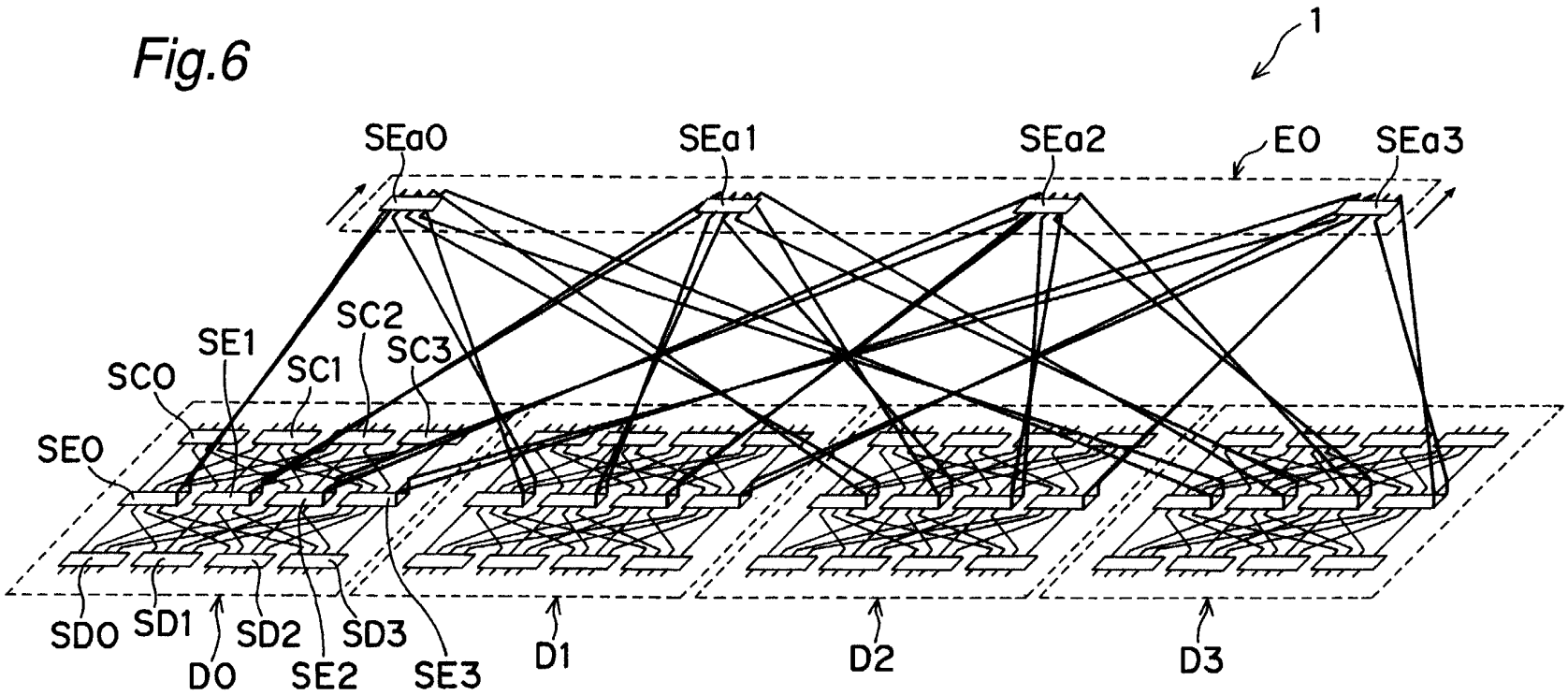
1
SEa0
SEa1
SEa2
EO
SEa3
SC2
SE1
SC3
SC1
SCO
SEO
SDO
SD1
SD2
SD3
DO
SE2
SE3
D1
D2
D3

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Fig.7

OUTPUT PORT NUMBER	CURRENT TIME	HOLD PORT	HOLD CLOCK	PORT DEMAND WAITING QUEUE	STATUS
#0	157843	#3	2	–	HOLD
#1	157843	–	0	#0,#2	RELEASE
#2	157843	–	0	#1	RELEASE
#3	157843	–	0	–	RELEASE

Fig.8

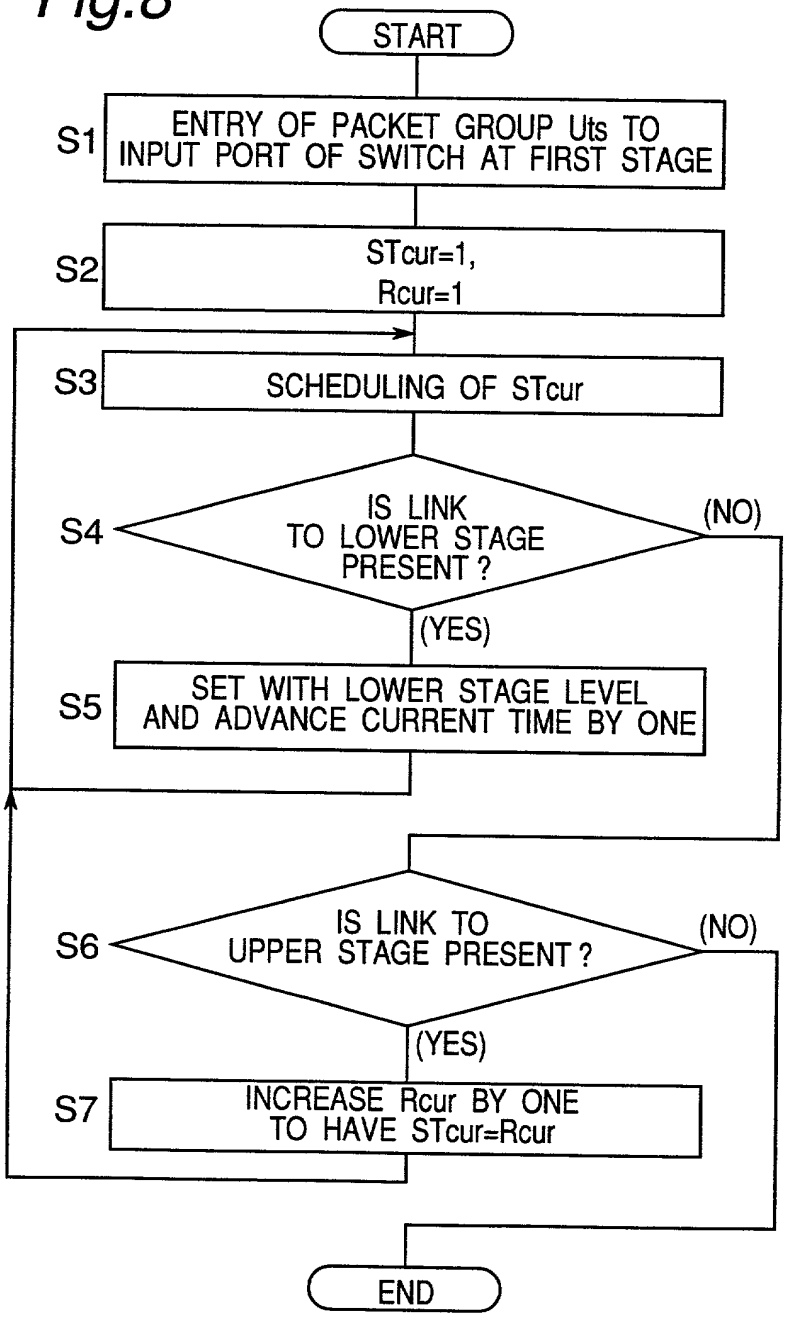

START
S1
ENTRY OF PACKET GROUP Uts TO INPUT PORT OF SWITCH AT FIRST STAGE
S2
STcur=1, Rcur=1
S3
SCHEDULING OF STcur
S4
IS LINK TO LOWER STAGE PRESENT ?
(NO)
(YES)
S5
SET WITH LOWER STAGE LEVEL AND ADVANCE CURRENT TIME BY ONE
S6
IS LINK TO UPPER STAGE PRESENT ?
(NO)
(YES)
S7
INCREASE Rcur BY ONE TO HAVE STcur=Rcur
END

Fig.9

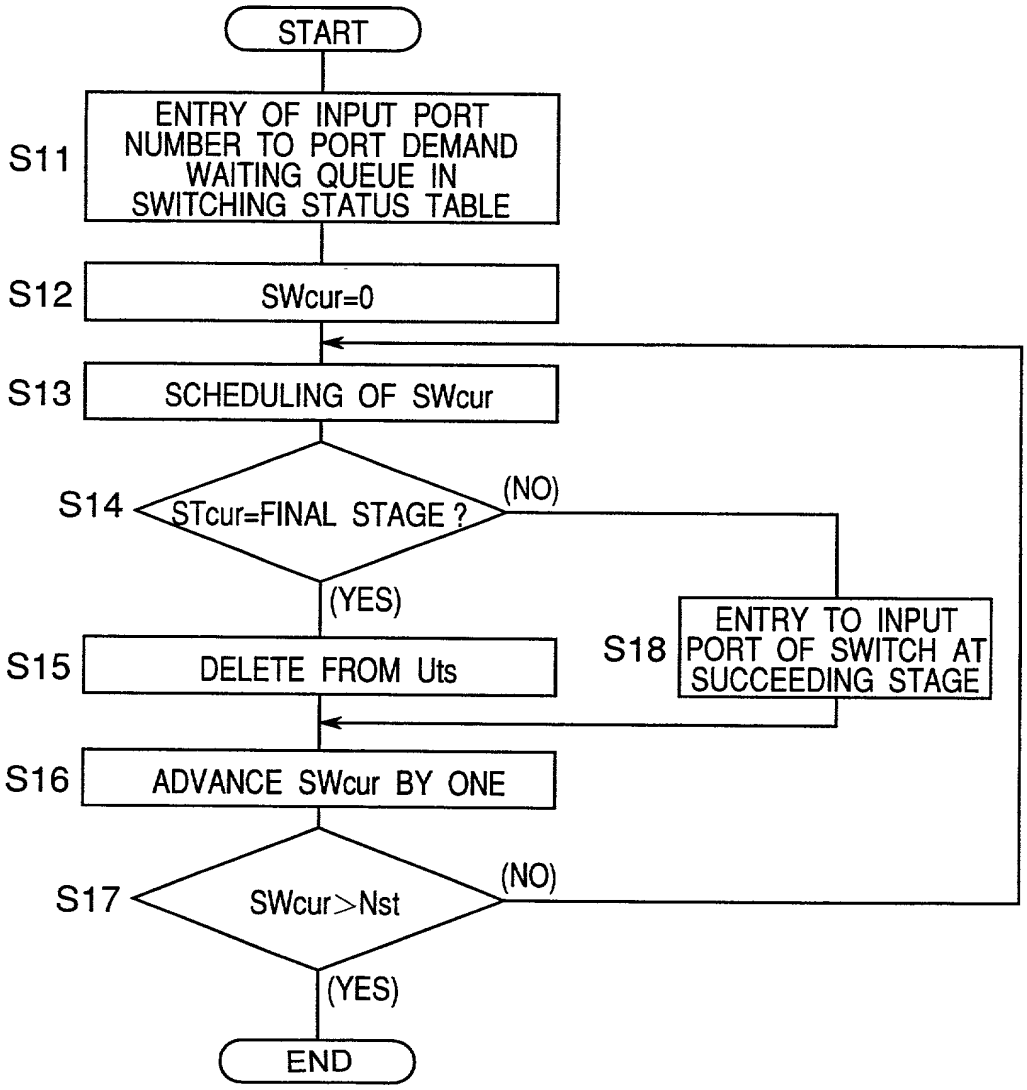

START
S11
ENTRY OF INPUT PORT NUMBER TO PORT DEMAND WAITING QUEUE IN SWITCHING STATUS TABLE
S12
SWcur=0
S13
SCHEDULING OF SWcur
S14
STcur=FINAL STAGE ?
(NO)
(YES)
S15
DELETE FROM Uts
S18
ENTRY TO INPUT PORT OF SWITCH AT SUCCEEDING STAGE
S16
ADVANCE SWcur BY ONE
S17
SWcur>Nst
(NO)
(YES)
END

Fig.10

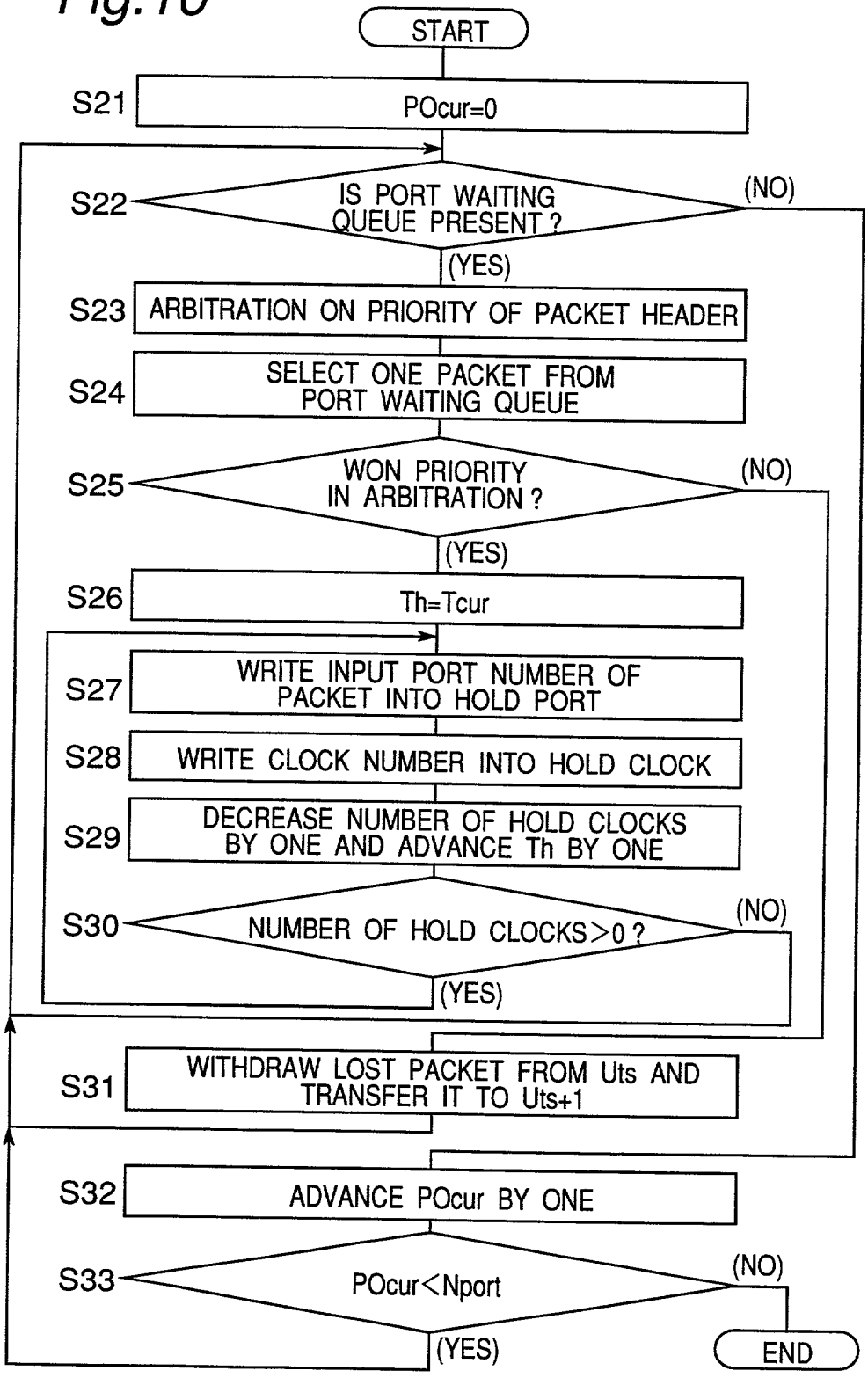

START
S21
POcur=0
S22
IS PORT WAITING QUEUE PRESENT ?
(NO)
(YES)
S23
ARBITRATION ON PRIORITY OF PACKET HEADER
S24
SELECT ONE PACKET FROM PORT WAITING QUEUE
S25
WON PRIORITY IN ARBITRATION ?
(NO)
(YES)
S26
Th=Tcur
S27
WRITE INPUT PORT NUMBER OF PACKET INTO HOLD PORT
S28
WRITE CLOCK NUMBER INTO HOLD CLOCK
S29
DECREASE NUMBER OF HOLD CLOCKS BY ONE AND ADVANCE Th BY ONE
S30
NUMBER OF HOLD CLOCKS>0 ?
(NO)
(YES)
S31
WITHDRAW LOST PACKET FROM Uts AND TRANSFER IT TO Uts+1
S32
ADVANCE POcur BY ONE
S33
POcur<Nport
(NO)
(YES)
END

Fig.11

OUTPUT PORT NUMBER	CURRENT TIME	HOLD PORT	HOLD CLOCK	PORT DEMAND WAITING QUEUE	STATUS
#0	15000	–	0	–	RELEASE
#1	15000	–	0	#0,#1	RELEASE
#2	15000	#4	2	#3	HOLD
#3	15000	–	0	–	RELEASE
#4	15000	–	0	#2	RELEASE

Fig.12

OUTPUT PORT NUMBER	CURRENT TIME	HOLD PORT	HOLD CLOCK	PORT DEMAND WAITING QUEUE	STATUS
#0	15000	–	0	–	RELEASE
#1	15000	#1	1	–	HOLD
#2	15000	#4	2	–	HOLD
#3	15000	–	0	–	RELEASE
#4	15000	#2	1	–	HOLD

Fig.13

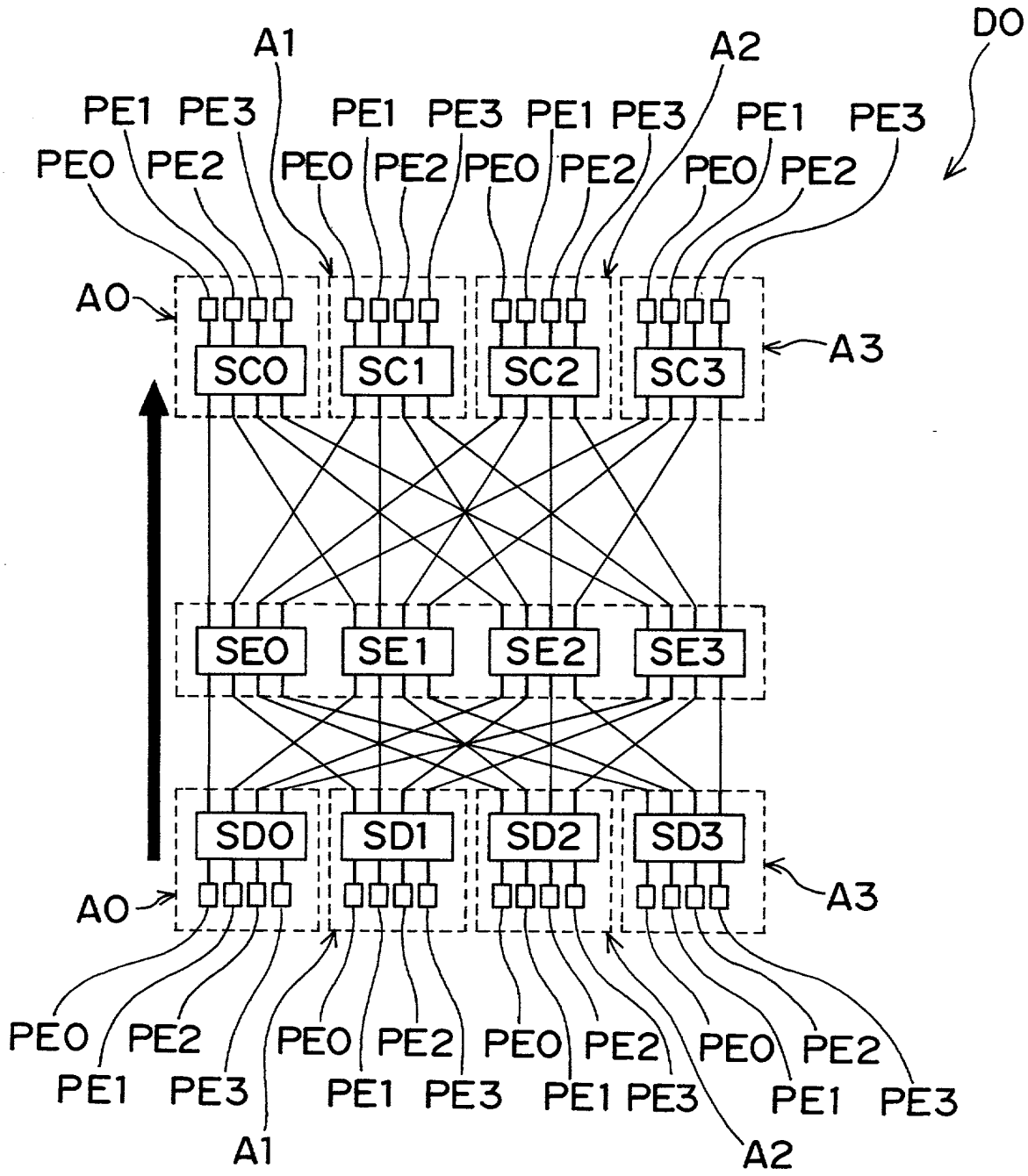

DO
A1
A2
PE1 PE3 PE1 PE3 PE1 PE3 PE1 PE3
PE0 PE2 PE0 PE2 PE0 PE2 PE0 PE2
A0
SC0 SC1 SC2 SC3
A3
SE0 SE1 SE2 SE3
SD0 SD1 SD2 SD3
A0
A3
PE0 PE2 PE0 PE2 PE0 PE2 PE0 PE2
PE1 PE3 PE1 PE3 PE1 PE3 PE1 PE3
A1
A2

Fig.14

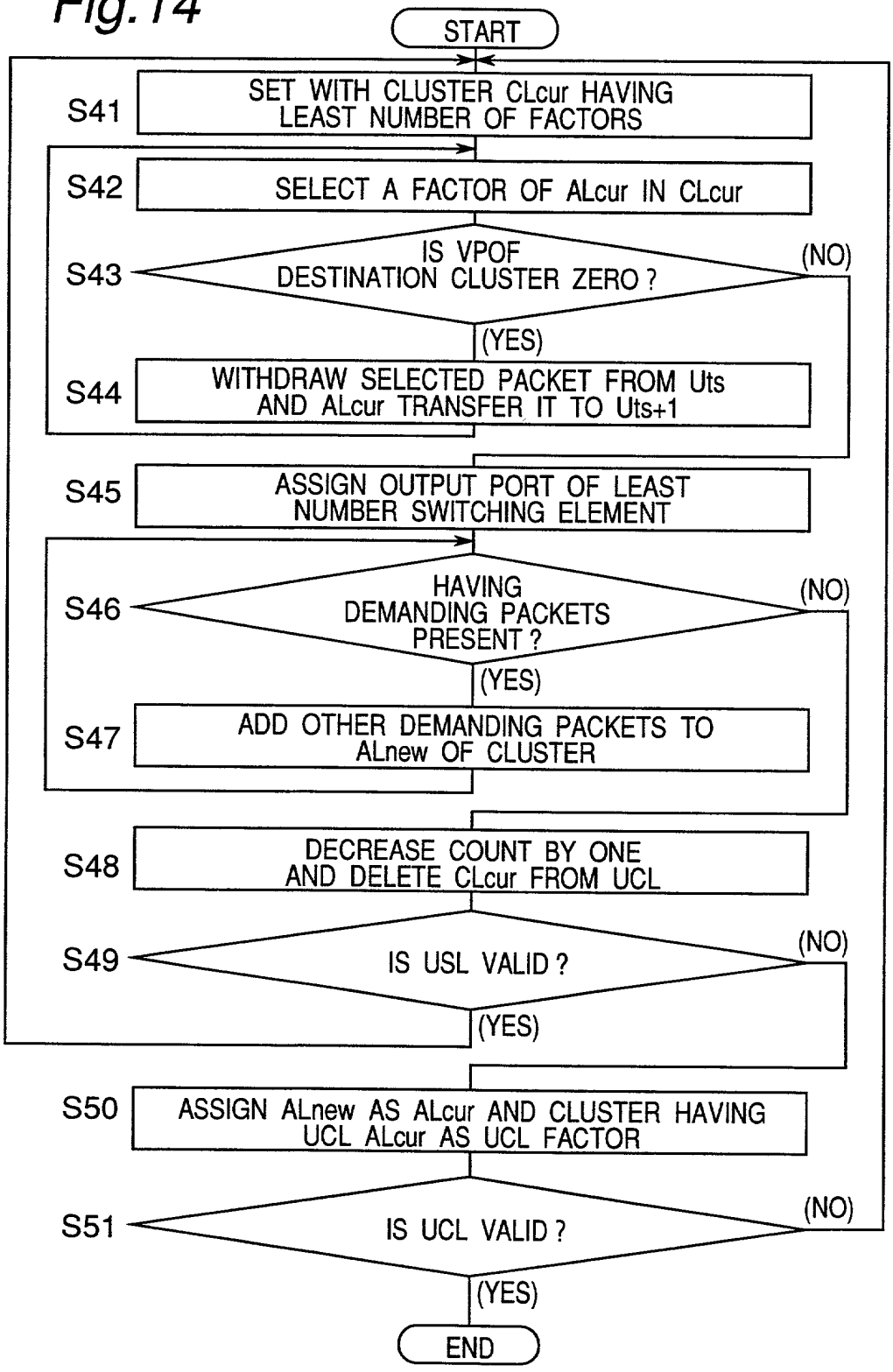

START
S41
SET WITH CLUSTER CLcur HAVING LEAST NUMBER OF FACTORS
S42
SELECT A FACTOR OF ALcur IN CLcur
S43
IS VPOF DESTINATION CLUSTER ZERO ?
(NO)
(YES)
S44
WITHDRAW SELECTED PACKET FROM Uts AND ALcur TRANSFER IT TO Uts+1
S45
ASSIGN OUTPUT PORT OF LEAST NUMBER SWITCHING ELEMENT
S46
HAVING DEMANDING PACKETS PRESENT ?
(NO)
(YES)
S47
ADD OTHER DEMANDING PACKETS TO ALnew OF CLUSTER
S48
DECREASE COUNT BY ONE AND DELETE CLcur FROM UCL
S49
IS USL VALID ?
(NO)
(YES)
S50
ASSIGN ALnew AS ALcur AND CLUSTER HAVING UCL ALcur AS UCL FACTOR
S51
IS UCL VALID ?
(NO)
(YES)
END

Fig.15

CLUSTER NUMBER	DESTINATION CLUSTER NUMBER
A0	A1,A3
A1	A2, A1, A1, A1
A2	A0,A1,A3
A3	A0,A2, A3

Fig.16

OUTPUT PORT NUMBER	#0	#1	#2	#3
COUNT	4	1	4	3

Fig.17

CLUSTER NUMBER	DESTINATION CLUSTER NUMBER
A0	A3
A1	—
A2	A0,A1
A3	A2

Fig.18

OUTPUT PORT NUMBER	#0	#1	#2	#3
COUNT	3	0	3	3

Fig.19

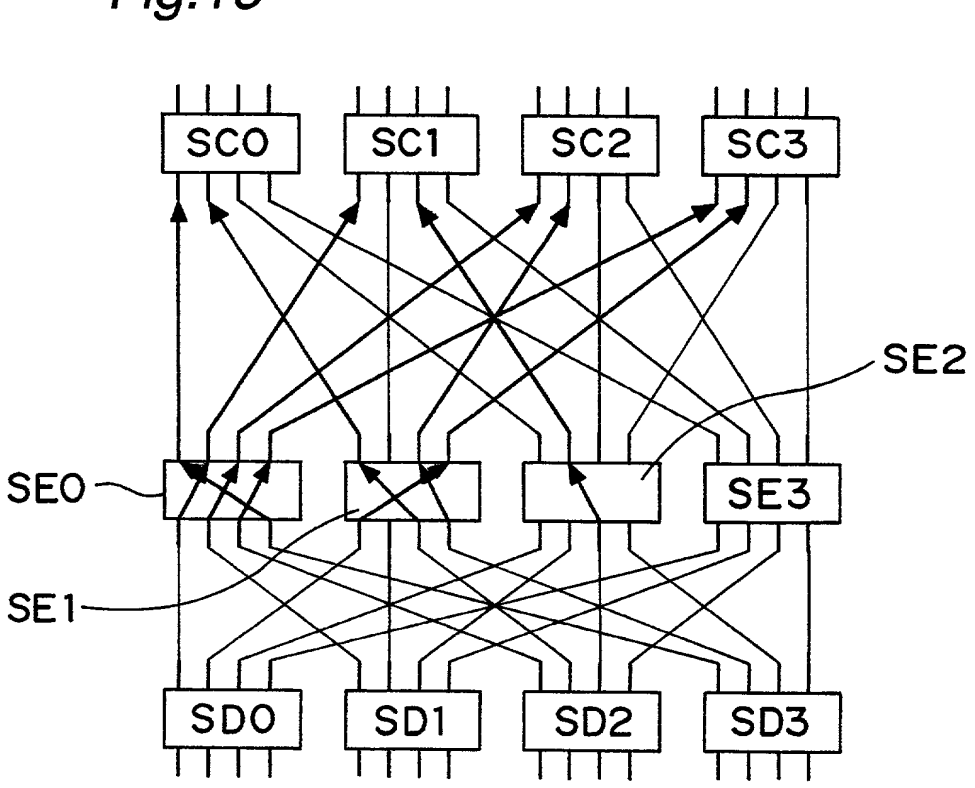


Fig.20

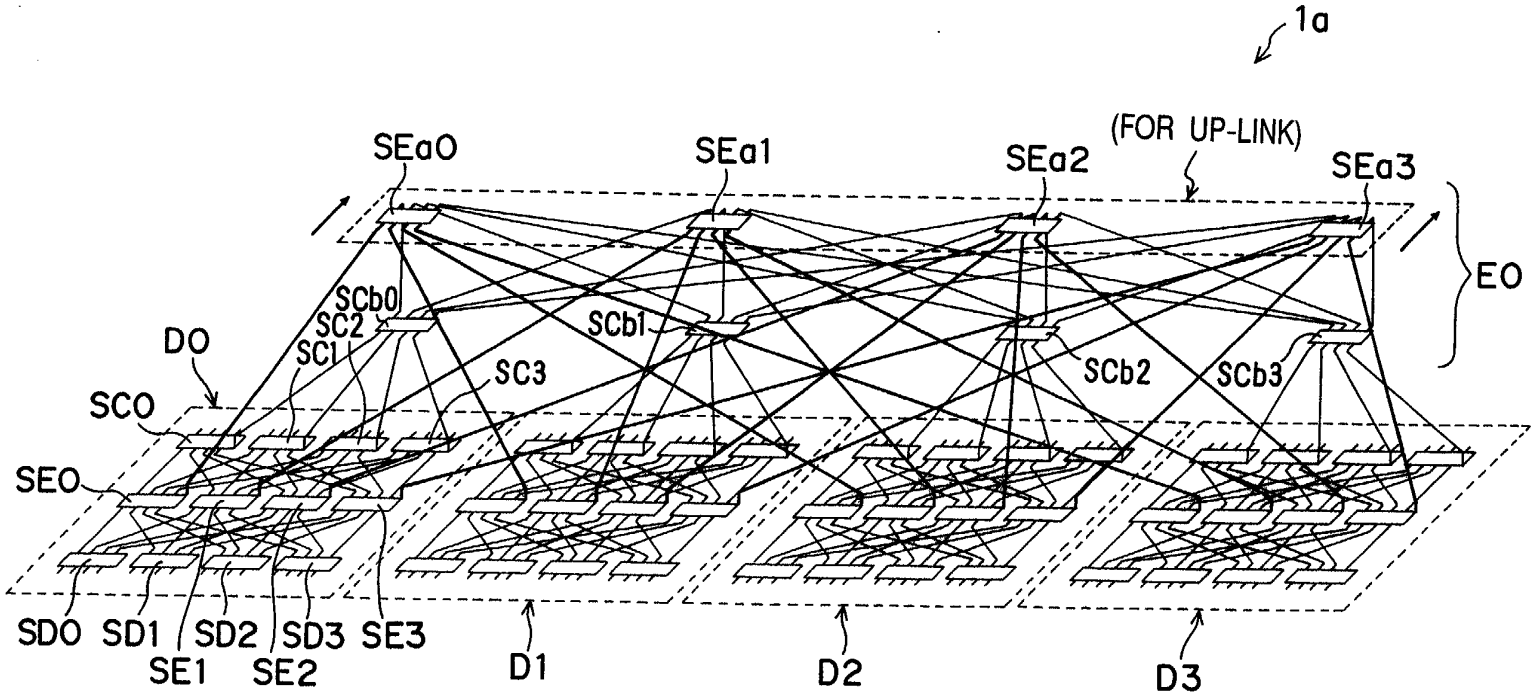

1a
(FOR UP-LINK)
SEaO
SEa1
SEa2
SEa3
EO
SCbO
SC2
SC1
DO
SCO
SEO
SC3
SCb1
SCb2
SCb3
SDO
SD1
SD2
SD3
SE3
SE1
SE2
D1
D2
D3

Fig. 21

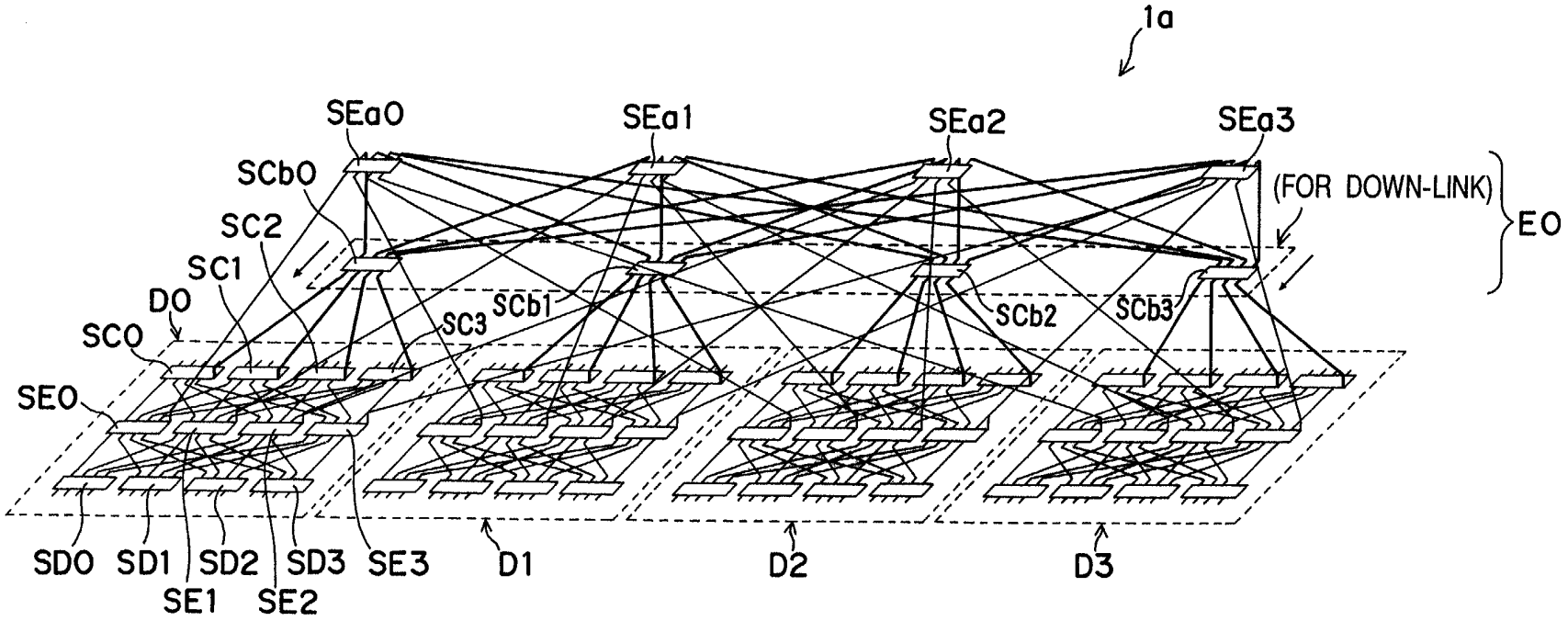

1a
SEa0
SEa1
SEa2
SEa3
SCb0
SC2
SC1
DO
SCO
SEO
SC3
SCb1
SCb2
SCb3
(FOR DOWN-LINK)
EO
SDO
SD1
SD2
SD3
SE3
SE1
SE2
D1
D2
D3

Fig. 22

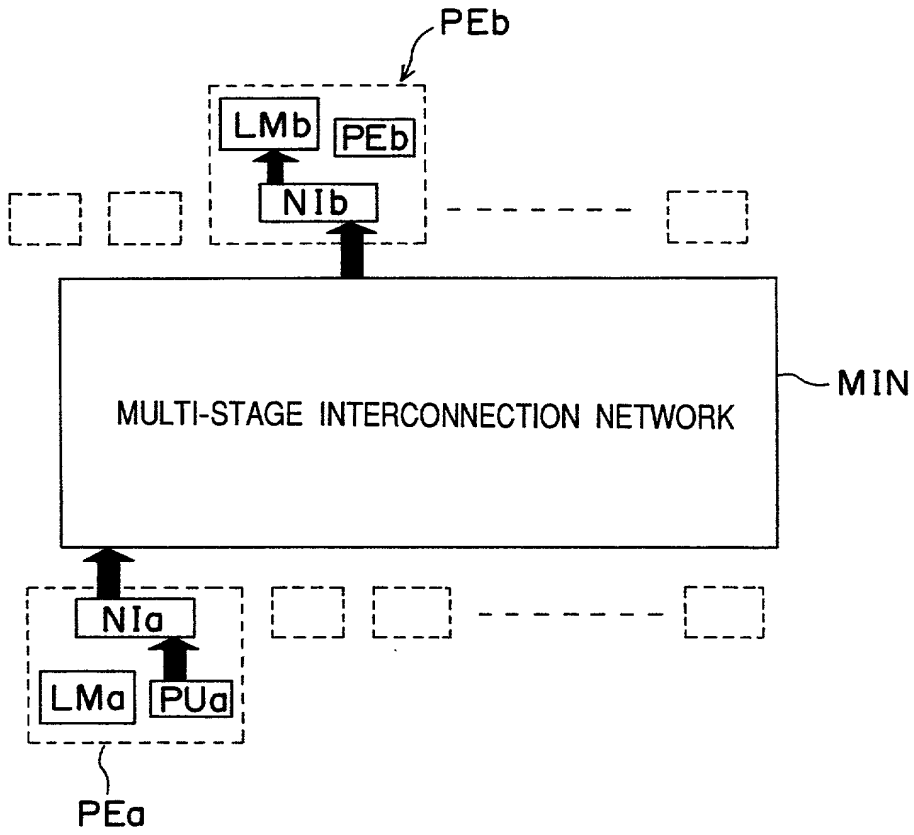
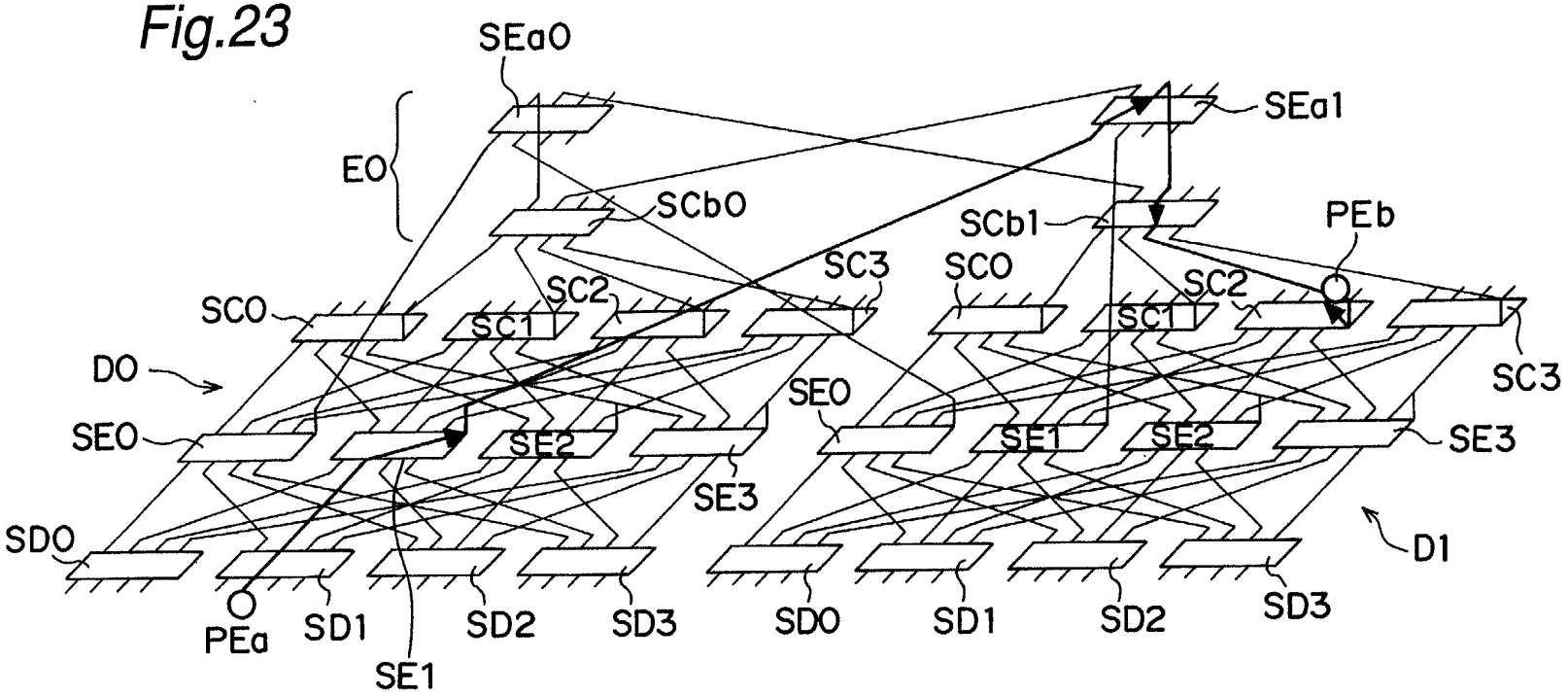

PEb
LMb
PEb
NIb
MULTI-STAGE INTERCONNECTION NETWORK
MIN
NIa
LMa
PUa
PEa

Fig.23


SEa0
SEa1
E0
SCb0
SCb1
PEb
SC0
SC1
SC2
SC3
DO
SE0
SE1
SE2
SE3
SD0
SD1
SD2
SD3
PEa
D1